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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,108	03/08/2001	Ashley Saulsbury	16747-017800	5576

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,108	SAULSBURY ET AL.	
	Examiner	Art Unit	
	William M. Treat	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-14,16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-9,11,13,14,16 and 18-24* is/are rejected.

7)☒ Claim(s) *10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-2, 4, 6-14, 16, and 18-24 are presented for examination.

2. Claims 11 and 13-14, 16, and 18-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The phrase, "connected to across bus across", in claims 11 and 23 makes no sense.

4. In line 22 of amended claim 13 applicants cite "said one or more processor chips" when the presumed antecedent for the phrase is "two or more processor chips" in line 3.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 6, 8-9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Tremblay (2001/0042187).

7. As to claim 1, Tremblay taught a processing core (100) comprising: R-number (two) processing pipelines (110, 112) each comprising N-number (four) of processing paths (220, 222), wherein each of said R-number (two) of processing pipelines (110, 112) are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of VLIW sub-instructions in parallel (p. 2, paragraph 15 and Fig. 5B) wherein each of said R-number of processing pipelines comprises S-number of register files such that said processing core comprises R x S-number of register files (p. 5, paragraph 52) and wherein each of said register files comprises Q-number of M-bit wide

registers (p. 5, paragraph 52) and wherein said Q-number of registers within each of said register files are either private or Global registers (p. 5, paragraph 52). and wherein when a value is written to one of said Q-number of said registers which is a Global register within one of said register files said value is propagated to a corresponding global register in the other of said register files(p. 5, paragraph 52) and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files said value is not propagated to a corresponding register in the other of said register files(p. 5, paragraph 52).

8. As to claim 2, Tremblay taught the processing core as recited in claim 1 wherein said R-number of processing pipelines can be configured to operate independently as separately operating pipelines (p. 2, paragraph 15).

9. As to claim 6, Tremblay taught the processing core as recited in claim 1, wherein a single VLIW processing instruction comprises R x N-number of P-bit sub-instructions appended together (p. 2, paragraph 15 and Fig. 5B). Inherently, Tremblay's sub-instructions are some value for P because without bits his instructions would not function.

10. As to claim 8, Tremblay taught the processing core as recited in claim (3) wherein said each of said R-number of processing pipelines comprise an execute stage which includes an execute unit for each of said N-number processing paths, each of said execute units comprising any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units (pp. 4-5, paragraphs 44, 48 and 49 and p. 14, paragraph 164 and Fig. 3).

11. As to claim 9, Tremblay taught the processing core as recited in claim 8 wherein an integer processing unit and a floating point processing unit share one of said register files (pp. 4-5, paragraphs 44, 48, 49, and 52 and p. 8, paragraph 81 and Fig. 3).

12. As to claim 11, Tremblay taught the processing core as recited in claim (5) wherein a plurality of said register files are connected to a bus, and a value written to a global register in one of said register files connected to the bus is propagated to a corresponding global register in the other of said register files connected to said bus across said bus (page 5, paragraph 52 and Fig. 4).

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay.

16. As to claim 7, Tremblay taught the processor chip as recited in claim 6 but did not specifically teach the chip wherein M=64, Q=64, and P=32. However, he taught such numerical values are a matter of design choice (p. 14, paragraph 164).

17. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (2001/0042187) in view of Rozenschein et al. (Patent No. 6,418,527).

18. Tremblay taught the invention of claim 1 from which claim 4 depends. (See paragraph 4, *supra*.) Applicants' claim 4 is for having multiple functional units within a pipeline share one register file as opposed to having individual register files (310, 312, 314, 316) for the functional units in a pipeline as taught by Tremblay. However, as Rozenschein teaches, having one or more register files in such a situation is a matter of design choice (col. 5, lines 5-8). Tremblay chose individual register files to provide faster access to data while a design which emphasized other considerations could chose the shared register file concept.

19. Claims 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. Applicant's arguments with respect to claims 1-2, 4, 6-14, 16, and 18-24 have been considered but are moot in view of the new ground(s) of rejection.

21. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER